ESOR ENGINEERING

EBERT 2904

Pulse Pattern Generator and Error Detector Datasheet

REV 1.0

2904 KEY FEATURES

- Four channel NRZ Pulse Pattern Generator and Error Detector
- Operating range between 24.6 to 29.5 Gb/s along with /2 rates
- Typical J_{RMS} of 1 ps and J_{PP} of 6 ps
- PRBS patterns of 2^7, 9, 15, 23, 31 and error insertion
- Non-destructive eye monitor
- Adjustable internal clock synthesizer with PPM offset control
- Adjustable clock output frequency and amplitude
- External clock input to synchronize parallel test systems
- Adjustable 200 to 1100 mV PP_{DIFF} output with squelch
- Adjustable Pre and Post cursor emphasis control
- TX and RX polarity inversion
- Loss of signal indicator
- 40 bit programmable fixed pattern
- USB 2.0 controlled with API command set or GUI software
- Stand alone configuration options available (consult the factory)
- Small footprint size of 216w x 60h x 140d mm
- Integrated cooling fan
- 1 year warranty

2904 DESCRIPTION

The 2904 is a high performance, flexible and cost effective four channel Pulse Pattern Generator (PPG) and Error Detector (ED) that can operate from 24.6 to 29.5 Gb/s along with half rates (consult factory for higher or lower operation). It is capable of generating a Pseudo Random Bit Sequence (PRBS) or a user defined 40 bit fixed pattern to test signal integrity of digital communication system links. PRBS patterns of 2^7, 9, 15, 23, 31 are supported. It is a standalone Bit Error Rate (BER) test solution that incorporates an internal full rate clock synthesizer therefore avoiding the expense of an external precision clock source.

Its small size allows it to be placed close to the Device Under Test (DUT) or further away using the TX driver pre and post emphasis controls features to compensate for cable and interconnect losses. It also has a non destructive integrated eye outline capture feature along with a quick eye height and width measurement capability.

It incorporates internal AC coupling capacitors on all ports to avoid CML bias issues and to protect the equipment along with the DUT. The PPG TX output has typical J_{PP} of ~6 ps and J_{RMS} of ~1 ps along with an adjustable range of 200 to 1100 mV PPDIFF providing a wide test range that could include crosstalk measurements. Other features include squelch, polarity inversion, loss of signal and error insertion.

The system is controlled through a USB 2.0 compliant port and supplied GUI to evaluate the performance of the system. An API command set is used for ease of integration into existing factory software automation control. The GUI includes a API tab so you can easily view the command architecture.

The 2904 accessories include: AC power cord, power supply, USB cable, GUI software and user manual.

Optional features: Tilt bar, custom power up configuration for standalone operation, parallel I/O control, dipswitch control, LED status diagnostics, individual PPG or ED configurations, face plate for 19 inch rack attachment, loopback cables or adding attenuators to the ED to adjust sensitivity.

2904 APPLICATIONS

The 2904 PPG and ED is a standalone test system or can be used in conjunction with other high speed test equipment for additional testing capability. Its capability to measure every bit of the incoming pattern is used as a tool to measure reliability and performance of communication links to determine BER over time or by changing parameters of the link. The PPG can be used by itself with a high bandwidth oscilloscope to measure a DUT's performance looking for common attributes associated with digital eye diagrams such as jitter. The ED can be used by itself as a receiver in a communication link to monitor the incoming pattern to determine the performance of a system where the source is physically located off-site.

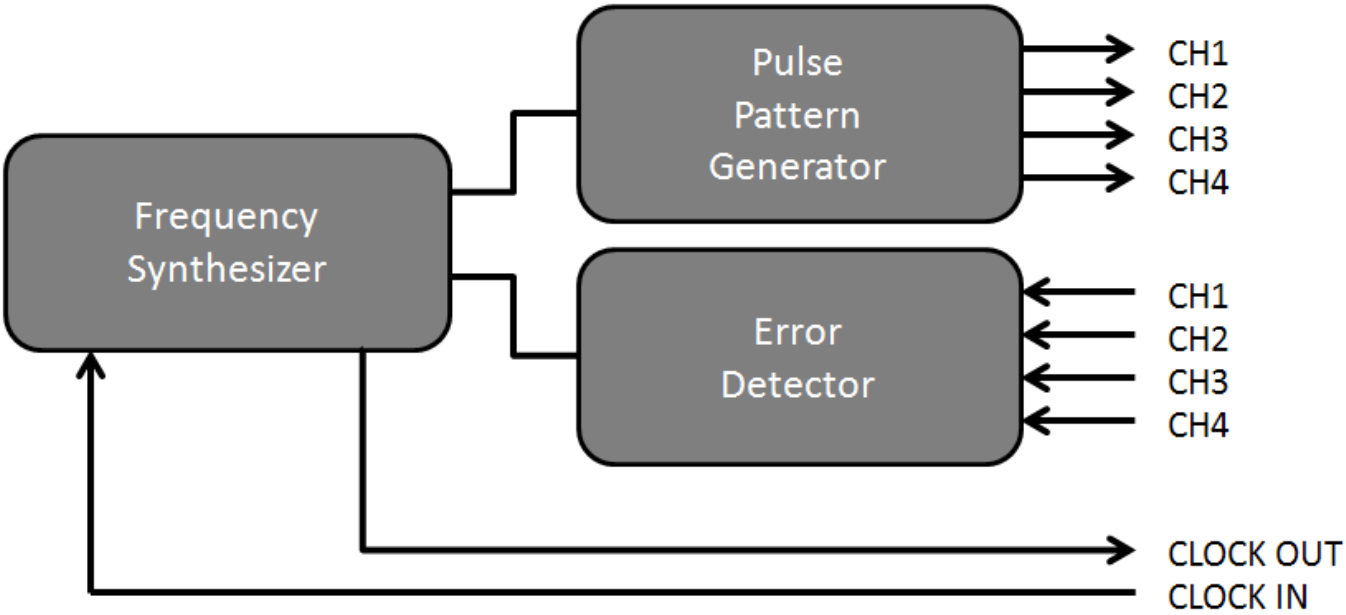
It has the capability of locking the synthesizer to an external clock source for use with other external test equipment or to run multiple 2904 systems in parallel to expand to higher port counts. The system has a PPM offset control feature to system tolerances or to adjust its aging over time.

The high fidelity performance also lends itself for testing in non-retimed links where the source needs to have low intrinsic jitter so it can be determined how much the DUT is contributing to the system link test. The ED has high sensitivity for applications that need this requirement or the use of external attenuators can be used to move the sensitivity to higher levels. Contact the factory if you would like to have the ED sensitivity changed to a higher level using a custom part number.

The eye capture feature also can give insight to the quality of the incoming digital signal such as eye width and shape It's not intended to replace a high speed scope, but can give you information about the eye symmetry and crossing width as the ED incorporates a limiting amplifier for increased sensitivity.

The 2904 was designed to characterize high speed digital links during the engineering, manufacturing or installation phases of a project. Such applications could include the testing of IC's, optical components, transceivers, copper cables, back planes and interconnects. The 2904 can be used for compliance testing of Ethernet, Fiber Channel, Infiniband, PCIE, SONET and proprietary link standards.

2904 ARCHITECTURE



2904 ELECTRICAL EYE DIAGRAMS

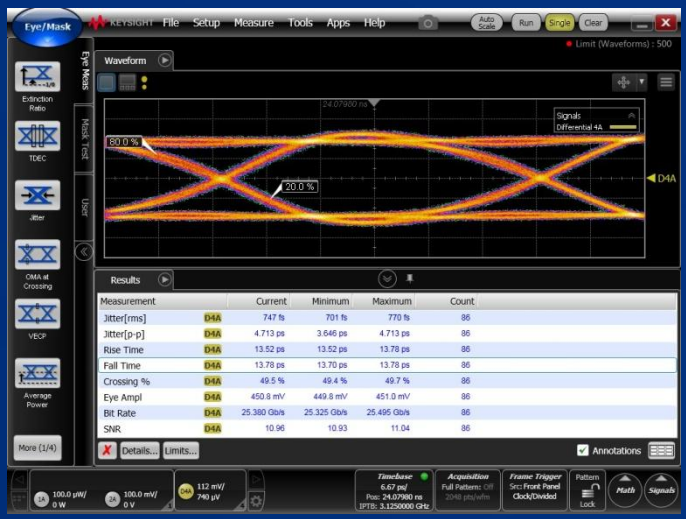
Typical Eye Diagram and measurement parameters at 26 Gb/s PRBS 2^31:

Typical Eye Diagram at 26 Gb/s using a precision timebase reference module PRBS 2^31:

2904 ELECTRICAL EYE DIAGRAMS

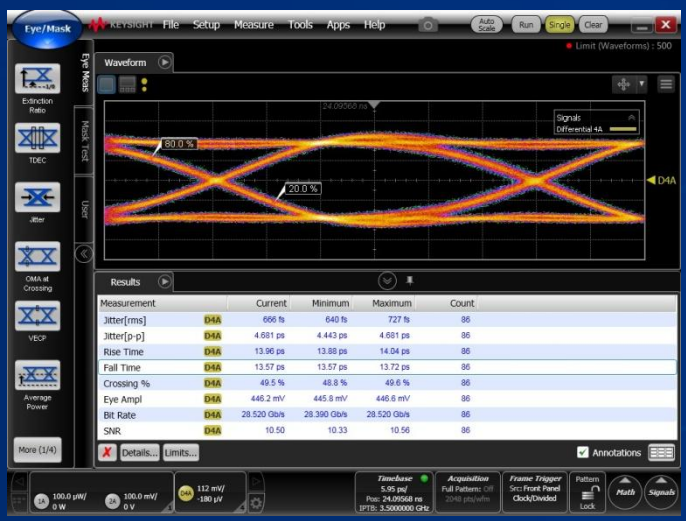
Typical Eye Diagrams using a precision timebase reference module PRBS 2^31:

25 Gb/s



27 Gb/s

28 Gb/s



29 Gb/s

2904 SPECIFICATIONS

Absolute Maximum Ratings	Symbol	Min.	Typ.	Max.	Unit	Notes
Storage Temperature	Ts	-20	–	70	°C	
AC Voltage Range	VAC	90	–	246	VAC	
AC Voltage Frequency Range	VFREQ	47	–	63	Hz	
Data RF Voltage Input	VinData	-0.3	–	1.2	V	
Clock In Voltage Input	VinClk	0	–	1.8	V	
USB Pin Voltage	VinUSB	-0.3	–	5.5	V	
RF and Clock ESD HBM	RFesdH	-1000	–	1000	V	
RF, Clock and USB Latchup	Vl	-100	–	100	mA	
USB ESD HBM	USBesdH	-2000	–	2000	V	
USB ESD CDM	USBesdC	-500	–	500	V	
Electrical Characteristics	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Notes**
Case Temperature	Tc	5	–	45	°C	
AC Supply Current	Icc	0.75	300	–	mA	
Baud Rate (NRZ format)	BR	12.3/14.75		24.6/29.5	Gb/s	
Baud Rate Setpoint Accuracy	BRa	-10	–	+10	PPM	(Note 1)
Baud Rate PPM Offset	BRo	-999	–	999	PPM	1 PPM step size
Power On Initialization Time	Ton	–	–	8	Seconds	
Eye Phase Steps	EMp	–	–	128	Steps	.31 pS per unit
Eye Amplitude Steps	EMv	–	–	64	Steps	6.25 mV per unit
Note 1: Aging, Temperature and Voltage						
TX Electrical	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Notes**
CML Output (Single Ended)	VoutSE	100	–	550	mVpp	AC Coupled
CML Output (Differential)	VoutDIFF	200	–	1100	mVpp	AC Coupled
CML Output (Differential) Step Size	VoutSS	–	5	–	mVpp	
CML Output (Differential) Squelch	VoutSqu	0	–	20	mVpp	
CML Output (Rise/Fall Time)	tR, tF	–	12	–	ps	20-80%
Output Impedance (differential)	Zout	–	100	–	Ω	
Termination Mismatch	TZm	–	–	5	%	
AC common mode voltage	TACcm	–	–	15	mVRMS	
Differential Return Loss	SDD22	-10	–	–	dB	
Jitter (RMS)	TJrms	–	1	–	pS	(Note 2)
Jitter (PK-PK)	TJpp	–	5	–	pS	(Note 2)
Pre-Emphasis Control	TPE	–	6	–	dB	
De-Emphasis Control	TDE	–	6	–	dB	
Note 2: Agilent DCA-X with 50 GHz plug-in, 23-1 PRBS pattern and 500 waveforms using a precision time base trigger						

2904 SPECIFICATIONS

RX Electrical	Symbol	Min.	Typ.	Max.	Unit	Notes
Baud Rate Tolerance	BRt	-100	–	+100	PPM	
CML Input Voltage (Single Ended)	VinSE	200	–	600	mVpp	AC Coupled
CML Input Voltage (Differential)	VinDIFF	100	–	1200	mVpp	AC Coupled
Input Impedance (Differential)	Zin	–	100	–	Ω	
Termination Mismatch	RZm	–	–	10	%	
Differential Return Loss	SDD11	-10	–	–	dB	
CDR Acquisition Lock Time	CDRl	–	–	500	mS	
Clock - Input	Symbol	Min.	Typ.	Max.	Unit	Notes
Frequency	CFin	156,248,438	156,250,000	156,251,562	Hz	Square wave
Single Ended Voltage Swing	CVpp	0.3	–	1.8	V	
Input Impedance	CRin	49.5	50	50.5	Ohm	AC coupled
Rise/Fall Time	CitR, CitF	–	–	1	nS	20%-80%
Duty Cycle	CDC	40	–	60	%	<1nS Tr/Tf
Random Jitter (RMS)	CRj	–	–	1	ps	12 kHz–20 MHz
Clock - Output	Symbol	Min.	Typ.	Max.	Unit	Notes
Clock Frequency	CF	0.096		3.6875	GHz	
Programmable Divider of Line Rate	CPDLR	8	–	256	/N	Factors of 2
Single Ended Voltage Swing	CVoutSE	200	–	400	mVp	AC coupled
Termination Mismatch	CZm	0	–	5	%	At 1 MHz
Rise/Fall Time	COtR, COtF	–	12	–	ps	20-80%
Ouptut Return Loss	CS22	-10	–	–	dB	
Jitter (RMS)	CJrms	–	–	750	fs	(Note 3)
Jitter (PK-PK)	CJpp	–	–	3.5	ps	(Note 3)
Note 3: Using Agilent DCA-X with 50 GHz plug-in. 500 waveforms using a precision time base trigger						
Note 4: Terminate clock output if not used						

2904 JITTER PHASE MEASUREMENTS

2904 TX Phase Jitter Measurements at 28.2 Gb/s using PRBS 2^15 - Part 1 of 2:

2904 TX Phase Jitter Measurements at 28.2 Gb/s using PRBS 2^15 - Part 2 of 2:

2904 JITTER AMPLITUDE MEASUREMENTS

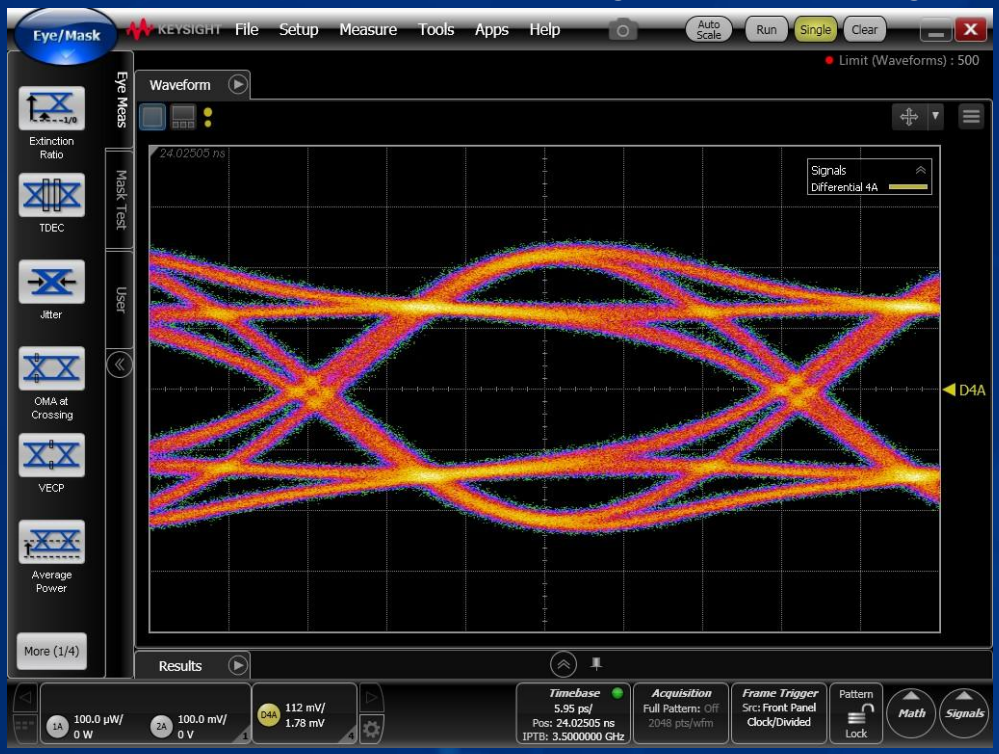
2904 TX Amplitude Jitter Measurements at 28.2 Gb/s using PRBS 2^15 - Part 1 of 2:

2904 TX Amplitude Jitter Measurements at 28.2 Gb/s using PRBS 2^15 - Part 2 of 2:

2904 ADDITIONAL JITTER AND EMPHASIS EXAMPLE

2904 TX Additional Jitter Measurements at 28.2 Gb/s using PRBS 2^15:

2904 TX Emphasis Example – 4dB Post Setting at 28.2 Gb/s using PRBS 2^31:



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